Data Sheet

SV32WB0xx Combo Connectivity MCU

Fully integrated Wi-Fi and BLE Combo SoC for IoT Applications

General Description

The SV32WB0xx is a fully integrated SoC with 2.4GHz band 1T1R 11b/g/n Wi-Fi, Bluetooth Low Energy 5.0, and MCU. A single chip MCU SoC targets for applications requiring optimal RF performance, strong security, low power consumption, and small form-factor with minimal external components. Equipped with a proven SDK, SV32WB0xx provides customers a fast time to market solution by leveraging existing software eco system, and still keep possibilities for product differentiation.

The SV32WB0xx supports BLE Master, Slave, Advertiser, Scanner roles concurrently. It also supports GATT and Mesh profile concurrently. The SV32WB0xx supports standard HCI in BLE side.

The SV32WB0xx integrates the Balun, T/R switch, LNA, PA with advanced architecture enhancement to achieve great receive sensitivity even in noisy home scenarios.

The SV32WB0xx's highly integrated on-chip Power Management Unit (PMU) support 3.3~5V wide range supply voltage switching regulators and LDOs to provide noise isolation between digital and analog domains, minimizing external Bill of Material (BoM). The innovated PMU architecture also covered flexible IO voltage to either 3.3V or 5V avoid expansive level shift in PCB circuit design, for example, 5V UART use case, SV32WB0x still provide I2C device 3.3V or 5V IO option to system level design consideration.

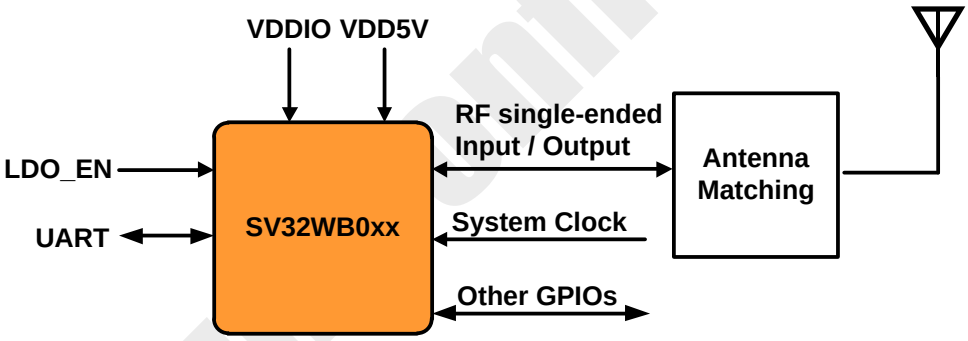
The SV32WB0xx features an application processor subsystem based on Andes D10F 32-bit RISC floating point core which runs at up to 480MHz. The chip includes up to 512KB of embedded SRAM, split among D10F's local TCMs and system SRAM. The entire 512KB SRAM is peripheral addressable. Dedicated 16KB instruction cache and 16KB data cache provides great performance for the execute-in-Place (XIP) in NOR Flash.

The SV32WB0xx has a built-in hardware crypto engine, a True Random Number Generator (TRNG), and a 2304b e-fuse block for storing chip-specific information. This combining with high efficiency security middleware library, including secure boot and Wi-Fi WPA3, the SV32WB0xx builds strong secure system products for smart home applications.

The SV32WB0xx has an average of 210uA DTIM3 current, 33mA Rx current, and 212mA Tx current. The highly power optimized SV32WB0xL demonstrates a low power capability with an average DTIM3 current 150uA.

SV32WB0xx Key Points

- IEEE 802.11 b/g/n compliant
- Bluetooth version 5.0
- TX power +20 dBm (at pin)
- RX sensitivity -97.5 dBm (at pin)
- Single power supply, range from 3.3 ~ 5V
- 5V/3.3V IO voltage option
- Security subsystem
  - AES/SHA/ECC HW crypto engine
  - 2304b e-fuse, TRNG, Secure boot
  - Wi-Fi Alliance WPA3 support
- CPU core speed up to 480MHz
- Internal SRAM up to 512KB
- Internal flash up to 4MB
- Extra PTA for external 2.4GHz RF coexistence, e.g. Zigbee
- Low power feature
  - DTIM3: 210uA
  - STA/AP: 55mA (Tx 3Mbps, Continue Rx, 2min average)
- Support 24/26/40 MHz crystal oscillator
- Support 32.768 KHz oscillator for RTC (QFN60 package)
- Internal 32.768 KHz RC clock with calibration
- Comprehensive audio interface, including I2S and PDM.
- ADC 12-bit, 1MSPS, up to 8 channel
- Package: QFN32, 4x4 mm, 0.4mm pitch
- Package: QFN40, 5x5 mm, 0.4mm pitch
- Package: QFN60, 7x7 mm, 0.4mm pitch
- Temperature range: -40°C to +85°C



SV32WB0xx System Block Diagram

Table 1: Comparison of Interface for SV32WB0xx series

Part Number	Chip Information					Interface												
	Package	CPU CLK	Embedded SRAM	Embedded Flash	GPIO	UART	I2C Master/Slave	SPI Master	SPI Slave	Data SPI Slave	PWM	ADC	I2S	PDMTx	PDMRx	SDIO	Flash	PSRAM
SV32WB01x	QFN32	320MHz	384KB	16Mb	14	3	1	1	1	1	8	5		1		1		
SV32WB01-T	QFN32	480MHz	512KB	16Mb	14	3	1	1	1	1	8	5		1		1		
SV32WB05	QFN40	320MHz	384KB	16Mb	19	3	2	2	1	1	8	6	1	1	2	1		
SV32WB06	QFN60	480MHz	512KB		36	3*	2	3	2	1	8	8	2	1	2	1	1	1
SV32WB07	QFN40	480MHz	512KB	32Mb	19	3	2	2	1	1	8	6	1	1	2	1		

*One of UART ports can support 5V voltage for SV32WB06x

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Revision History

Version	Date	Description
0.1	2020/10/20	Draft
0.2	2020/10/21	• Deleted WMM PS • Modified System power consumption
0.3	2020/12/07	• Deleted SMAC description • Deleted SV32WB02x/SV32WB03 description • Modified Key Points description • Modified ch.1.5 SYSTEM description • Modified DTIM3 average current • Modified System power consumption • Modified Temperature range • Modified HOST Interface description • Modified Mode Selection table • Added BLE Function • Added ch.2.4 Power-on Sequence • Added ch.3 Interface Description • Modified Table 9: ESD Specifications • Modified Table 6: Absolute Maximum Ratings • Modified Table 14: Greenfield changed to Mixed mode • Modified Table 28: IOT ADC Pin Location • Modified ch.10Ordering Information • Modified Table 11: Recommended Operating Conditions and DC Characteristics • Modified Table 12, Table 13 for Frequency value and OSCIN Input Voltage Max. • Modified Table 16,Table 17
0.4	2021/01/21	• Added SV32WB03x and SV32WB06x • Modified Table 16
0.5	2021/03/31	• Added DataSPI Slave • Modified Figure 2: SV32WB0xx typical Power Connection • Modified Table 11: Recommended Operating Conditions and DC Characteristics • Modified Table 14: 2.4G WLAN RF Performance Specifications: Added Rx Sensitivity (HT40)
0.6	2021/06/11	• Added I/O current Description • Modified Table 16/Table 17: OFF mode current • Added SV32WB05x • Add 105°C part number • Delete SV32WB03 part, add SV32WB01-T part
0.7	2021/06/22	• Added SV32WB07x part • Delete SV32WB05L,SV32WB06L
0.8	2021/08/26	• Add GND E-PAD at each package
0.9	2021/09/13	• Fixed chapter 10 typo
0.91	2021/09/27	• Modified Chapter 2.4 reset timing duration to T2
0.92	2021/10/13	• Correct table 27 Pinmux Description for SV32WB0xx
1.0	2021/11/03	• Release • Modify figure 17: QFN 5x5 package dimensions

1.1	2022/01/20	• Corrected Table 1: Comparison of Interface for SV32WB0xx series • Corrected Table 6: Absolute Maximum Ratings • Modified Table 11: Recommended Operating Conditions and DC Characteristics

Table of Contents

Lists of Tables

Lists of Figures

1 System Overview

1.1 System Block Diagram

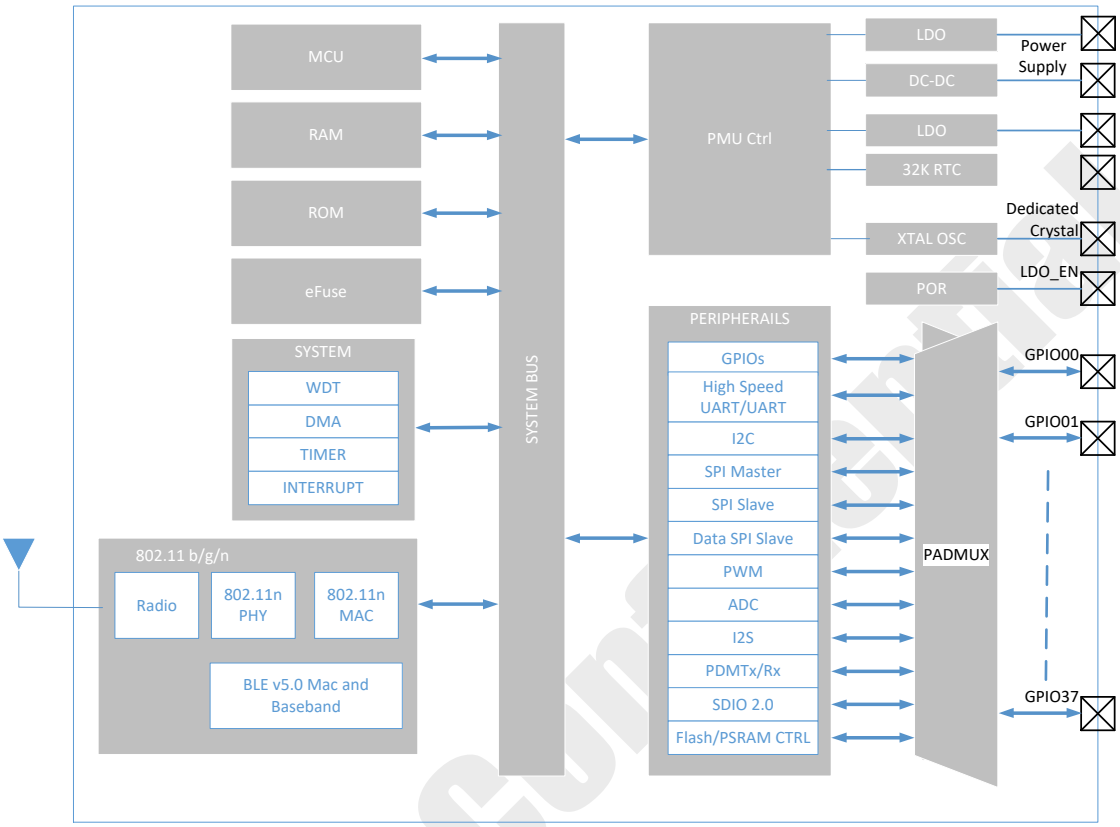


Figure 1: SV32WB0xx Block Diagram

1.2 General Description

The SV32WB0xx WLAN SoC is designed to support IEEE 802.11 b/g/n single spatial stream and Bluetooth 5.0. It is designed with the state of-the-art techniques and process technology to achieve low power consumption and high throughput performance to address the requirement of mobile and handheld devices. The SV32WB0xx WLAN low power function uses the innovative design techniques and the optimized architecture which best utilizes the advanced process technology to reduce active and idle power, and to achieve extreme low power consumption at sleep state to extend the battery life. The SV32WB0xx WLAN A-MPDU Tx function maximizes the throughput performance while achieving the best buffer utilization.
The Bluetooth subsystem contains the Bluetooth radio, baseband modem, and link controller.

1.3 WLAN FEATURES

- IEEE 802.11 b/g/n 1T1R compliant
- IEEE 802.11 d/e/i/k/r/w supported
- Support 20/40MHz up to MCS7 150Mbps
- 802.11n features supported
  - A-MPDU Tx & Rx for high MAC throughput
  - Support immediate Block-Ack
- STA, SoftAP and Sniffer modes supported
- Concurrent AP + STA supported
- Ad-hoc, peer-to-peer and Wi-Fi Direct modes supported
- Low power Tx/Rx for short range scenario
- Low power beacon listen mode
- Low power dormant mode
- WFA features
  - WEP/WPA/WPA2/WPA3
  - WMM
- Short Guard Interval for 802.11n optimal performance
- Greenfield mode for 802.11n optimal performance
- STBC in RX mode
- Tx power: +20 dBm
- Rx sensitivity: -97.5 dBm
- Integrated Balun, T/R switch, LNA and PA for 2.4GHz
- Enhanced and robust sensitivity for wider coverage range
- Supports calibration algorithm to handle non-ideal effects from CMOS RF block

1.4 BLUETOOTH FEATURES

- Bluetooth 5.0 Low Energy
- Integrated Balun and PA
- High power mode: up to 10 dBm
- Rx sensitivity: -94 dBm
- Channel assessment for AFH
- Internal co-existence scheme between Wi-Fi and Bluetooth
- Concurrently slave/advertiser/scanner operations supported
- Master mode supported
- SIG Mesh v1.01 supported
- GATT and Mesh profile
- Data channel long packet supported
- Device Provision Protocol (DPP) with BLE 5.0 Extended Advertising supported

1.5 SYSTEM

- Andes Technology D10F processor w/ ILM/DLM and I-cache/D-cache
- DSP instruction set with SIMD
- Tightly coupled single precision floating point unit (FPU)
- Dedicated 16KB I-cache/D-cache supported
- Memory Protection Unit (MPU) supported

- 128KB ROM and up to 512KB SRAM for Instruction and data SRAM in total
- Low power Dormant mode with 16KB retention SRAM
- Low power Shut-Down mode
- Integrated on-chip Power Management Unit (PMU) support 3.3~5V wide range
- 5V-tolerant fast IOs for dedicated pin, and multiple IO voltages supported
- Security and encryption
- AES/SHA/ECC hardware acceleration
- Integrated True Random Number Generator
- Integrated 2304b e-fuse and Secure boot
- Integrate flash up to 32Mb in the package
- Suspend/Wake-up manger controller
- 2 DMA, each with 8 channels
- Flash controller supports eXecute-in-Place (XIP)
- I2C Master/Slave
- 12-bit ADC for IOT
- Eight PWMs
- Four millisecond timers
- Four microsecond timers
- Two watchdog timers
- All pins can be multiplexed to GPIO by user scenario
- I2S
- PDM Tx/Rx

1.6 HOST INTERFACE

- High Speed UART
  - Support RX/TX/RTSN/CTSN, 4 pins
  - Baud rate up to 4.8 Mbps
- UART
  - Support RX/TX, 2 pins
  - Baud rate up to 921600 bps
- SDIO 2.0
  - 1bit/4bits mode supported
  - Support Clock up to 50MHz
- Data SPI Slave
  - Need a gpio as RX interrupt

1.7 SYSTEM CLOCKING AND RESET

The SV32WB0xx has a system clocking block and reset which controls the clocks and power going to other internal modules. Its inputs consist of sleep requests from these modules and its outputs consist of clock enable and power signals which are used to gate the clocks going to internal modules. The system clocking and reset block also manages resets going to other modules within the device.

1.8 DESIGN FOR TEST

It also has features which enable testing of digital blocks via ATPG scan, memories via MBIST, analog components, and the radio.

2 POWER SUPPLIES AND POWER MANAGEMENT

2.1 GENERAL DESCRIPTION AND PMU POWER CONNECTION

The power management unit (PMU) contains Low Dropout Regulators (LDOs), buck DC-DC converter and reference bandgap circuit.

The PMU integrates multi-LDOs and one buck converter. Those circuits are optimized for the given functions by balancing quiescent current, dropout voltage, line / load regulation, ripple rejection and output noise.

The input voltage of the buck converter is 3.3V. Its output voltage is 1.1V and feeds into the input power of the RF circuit and DLDO which has 0.8V output voltage for all digital circuits.
Figure 2 shows the typical power connection for SV32WB0xx. DLDO and some RF circuits are powered by the buck converter output. The VDDIO is a power input which may be 1.8V or 3.3V from the host side. The connection structure is shown in the Figure 2.

SV32WB0xx supports 5V input, and internal LDO generates 3.3V through RVD33_OUT for all 3.3V power pins. Figure 3 shows 5V power connection for SV32WB0xx. This feature can save one additional LDO component on PCB. The connection structure is shown in the Figure 3

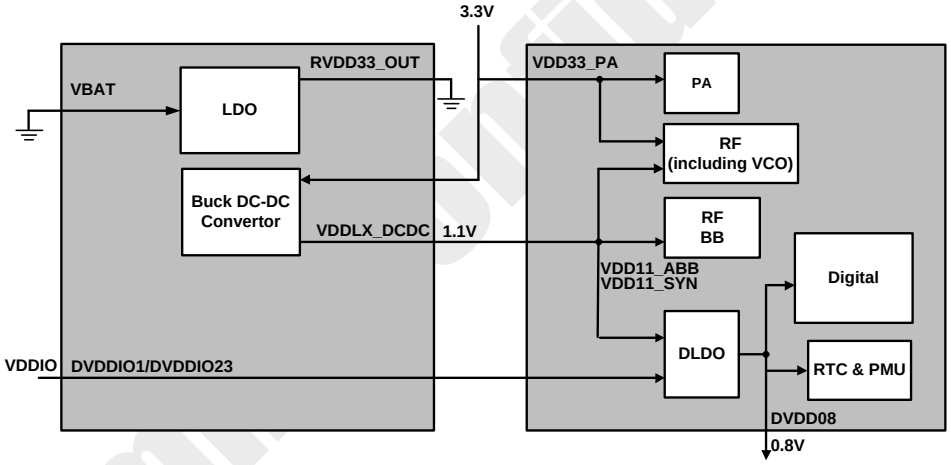


Figure 2: SV32WB0xx typical Power Connection

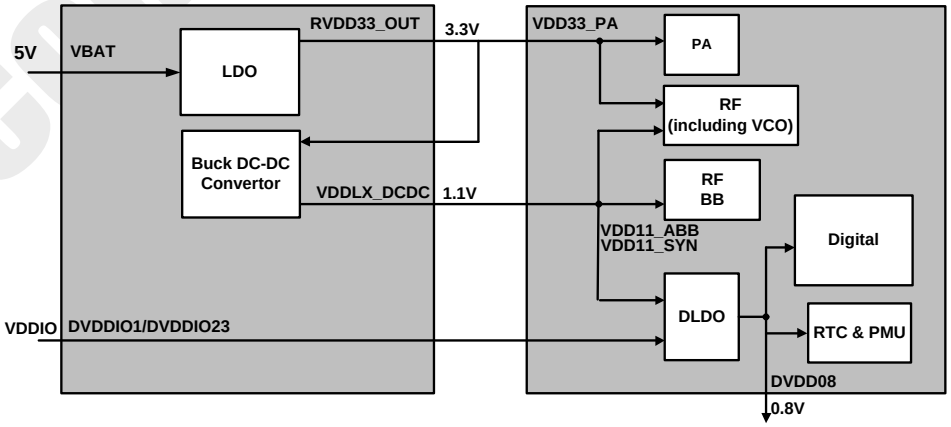


Figure 3: SV32WB0xx Power Connection with Internal LDO

2.2 DLDO

The DLDO is integrated in the PMU to supply digital core. It converts voltage from 1.1V input to 0.8V output which suits the digital circuits. The input is typically connected to the buck's output.

2.3 BUCK CONVERTER

The regulator is a DC-DC step-down converter (buck converter) to source 300mA (max.) with 1.3V to 1.05V programmable output voltage based on the register setting. It supplies power for the RF circuit and DLDO.

2.4 POWER-ON SEQUENCE

2.4.1 POWER-ON SEQUENCE WITH TYPICAL POWER

Figure 4 shows the VDD33=3.3V power-on sequence of the SV32WB0xx from power-up to firmware download, including the initial device power-on reset evoked by LDO_EN signal. The LDO_EN input level must be kept above the threshold voltage. After initial power-on, the LDO_EN signal can be held low to turn off the SV32WB0xx or pulsed low to induce a subsequent reset.

After LDO_EN is asserted, the host starts the power-on sequence of the SV32WB0xx. From that point, the typical SV32WB0xx power-on sequence is shown below:

1. Within T1+2.5ms, the internal power-on reset (POR) will be done. And host could download firmware code of DPLL setting if the crystal is not default setting, 26MHz. The internal running clock is crystal frequency.
2. After 100us of DPLL settling time, host could set internal clock to full speed and finish all the downloading of firmware code.

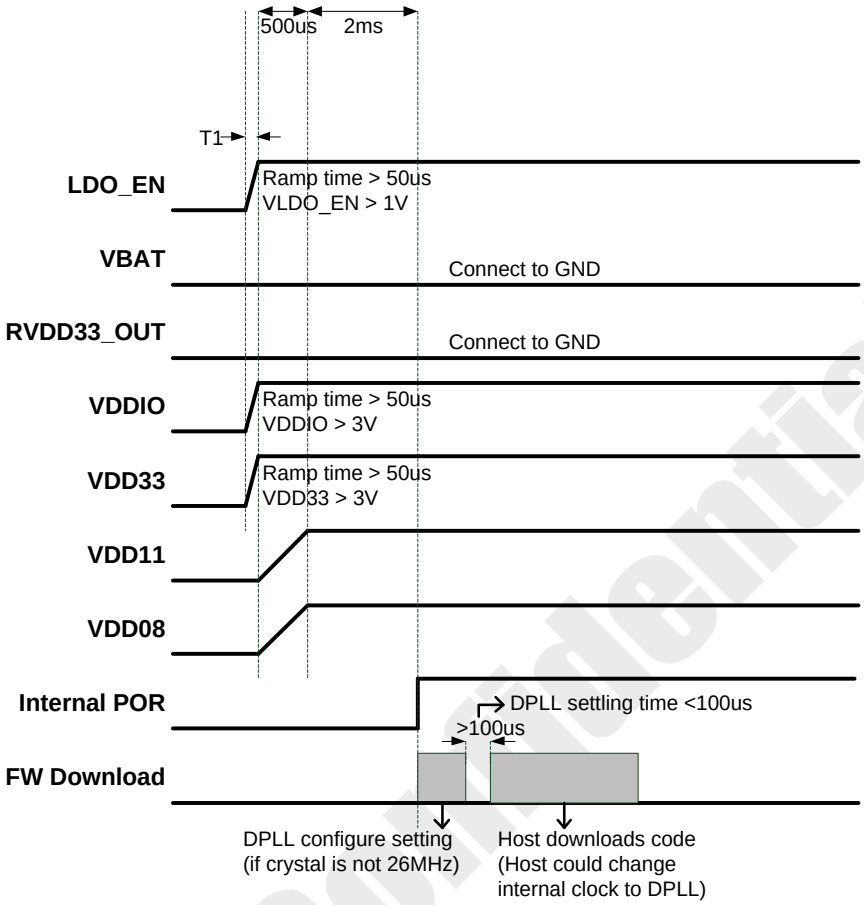


Figure 4: Power-on sequence with typical power

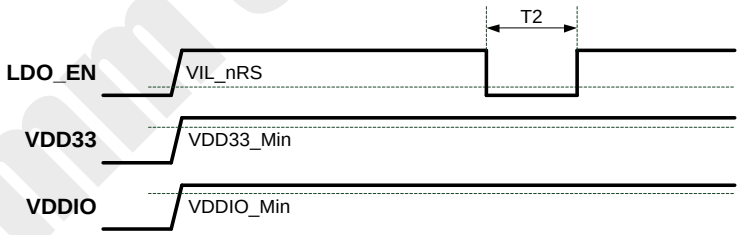


Figure 5: Reset Timing with typical power

2.4.2 Power-on Sequence with Internal LDO

Figure 6 shows the VBAT=5V power-on sequence of the SV32WB0xx from power-up to firmware download, including the initial device power-on reset evoked by LDO_EN signal. The LDO_EN input level pull high automatically by chip internal VBAT when VBAT input. After initial power-on, the LDO_EN signal can be held low to turn off the SV32WB0xx or pulsed low to induce a subsequent reset.

After LDO_EN is asserted. The host starts the power-on sequence of the SV32WB0xx. From that point, the typical SV32WB0xx power-on sequence is shown below:

1. Within T1+3.5ms, the internal power-on reset (POR) will be done. And host could download firmware code of DPLL setting if the crystal is not default setting, 26MHz. The internal running clock is crystal frequency.
2. After 100us of DPLL settling time, host could set internal clock to full speed and finish all the downloading of firmware code.

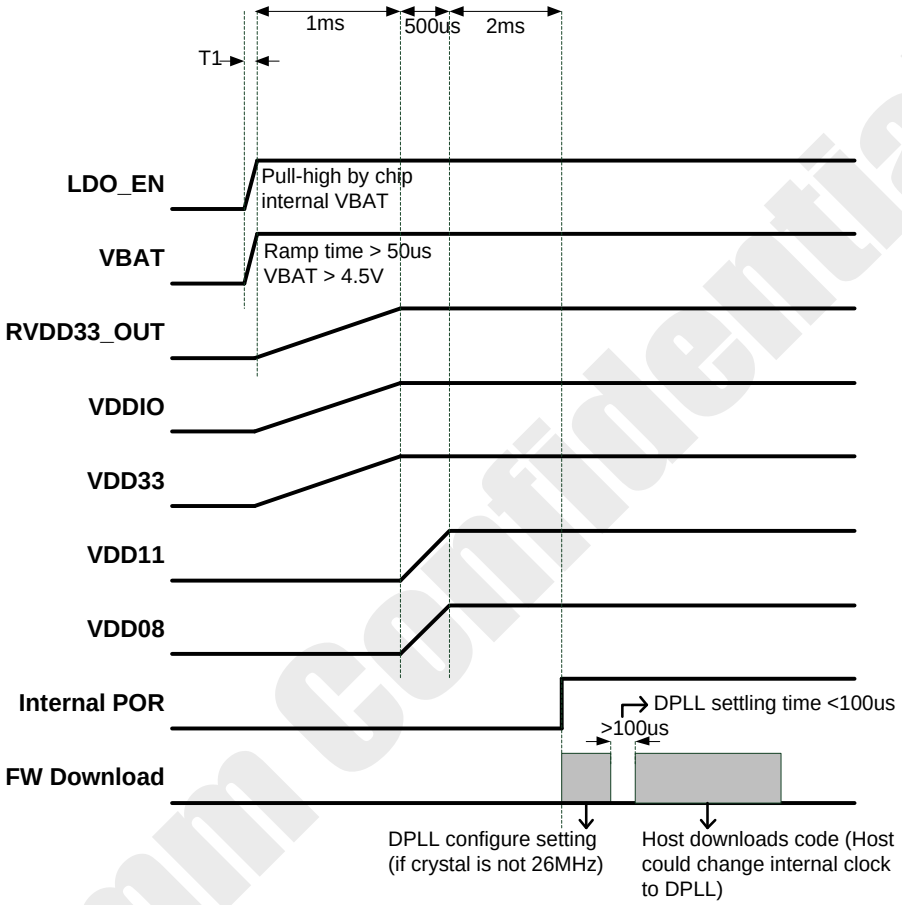


Figure 6: Power-on sequence with Internal LDO

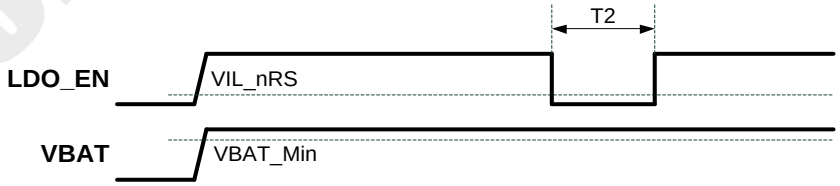


Figure 7: Reset Timing with Internal LDO

Table 2: Reset Timing Parameters

Parameters	Description	Min.	Unit
T_2	Duration of LDO_EN signal level < VIL_nRST (refer to its value in Table 11: Recommended Operating Conditions and DC Characteristics) to reset the chip	500	us

2.5 RESET CONTROL

The SV32WB0xx **LDO_EN** pin can be used to completely reset the entire chip. After this signal has been de-asserted, the SV32WB0xx is in off mode waiting for host communication. Until then, the MAC, Baseband modem, and MCU subsystem blocks are powered off and all modules are held in reset. Once the host has initiated communication, the SV32WB0xx turns on its crystal and later on DPLL. After all clocks are stable and running, the resets to all blocks are automatically de-asserted.

3 INTERFACE DESCRIPTION

3.1 SDIO CHARACTERISTICS

SDIO is compliant to SDIO specification version 2.0, supporting 1-bit and 4-bit data transfer mode, and compliant to high speed SD Bus.

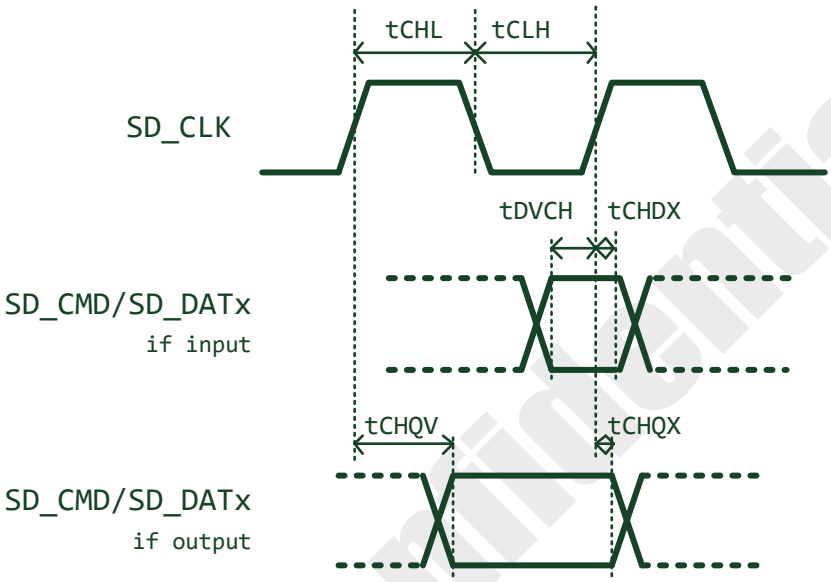


Figure 8: SDIO Timing

Table 3: SDIO Timing Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
SDIO clock frequency	–	(TBD)		50	MHz
SDIO clock high time	tCHL	7	–	-	ns
SDIO clock low time	tCLH	7	-	-	ns
SDIO input setup time	tDVCH	6	-	-	ns
SDIO input hold time	tCHDX	2	-	-	ns
SDIO output delay	Min.: tCHQX, Max.: tCHQV	2.5	-	14	ns

3.2 SPI Master Characteristics

The device features up to 3 SPI Masters that communicate in Full-duplex or Half-duplex (in either direction) mode. The SPI Master can be configured in any clock polarity (CPOL=0/1) and data phase (CPHA=0/1) combinations. The interface SCLK is divided from AHB clock, and supports frequency up to 20MHz. The interface input/output data could source from/sink to SRAM through DMA.

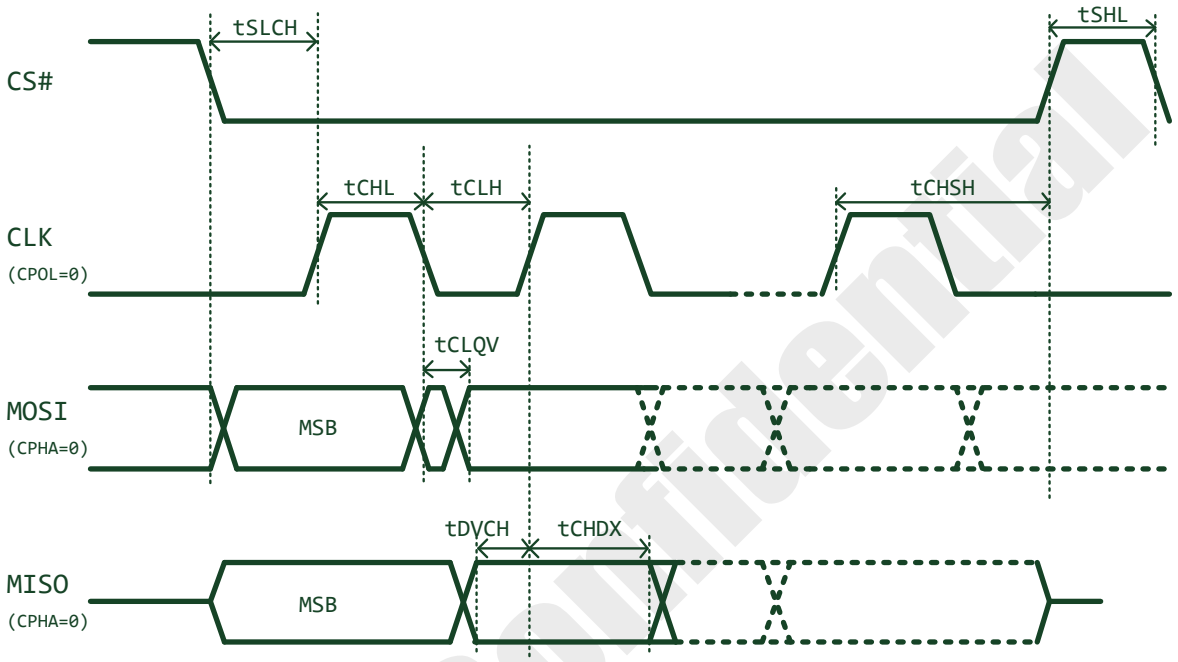


Figure 9: SPI Master Timing

Table 4: SPI Master Timing Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
SPI Master clock frequency	Clock divided by AHB clock	-	-	20	MHz
SPI Master clock high time	tCHL	22.5	–	-	ns
SPI Master clock low time	tCLH	22.5	-	-	ns
SPI Master CS# hold time	tCHSH	1T CLK	–	-	ns
SPI Master CS# setup time	tSLCH	0.5T CLK	-	-	ns
SPI Master CS# inactive time	tSHL	1T CLK			ns
SPI Master data in setup time	tDVCH	12	-	-	ns
SPI Master data in hold time	tCHDX	0	-	-	ns
SPI Master data output delay	tCLQV	-	-	2	ns

3.3 DATA SPI SLAVE CHARACTERISTICS

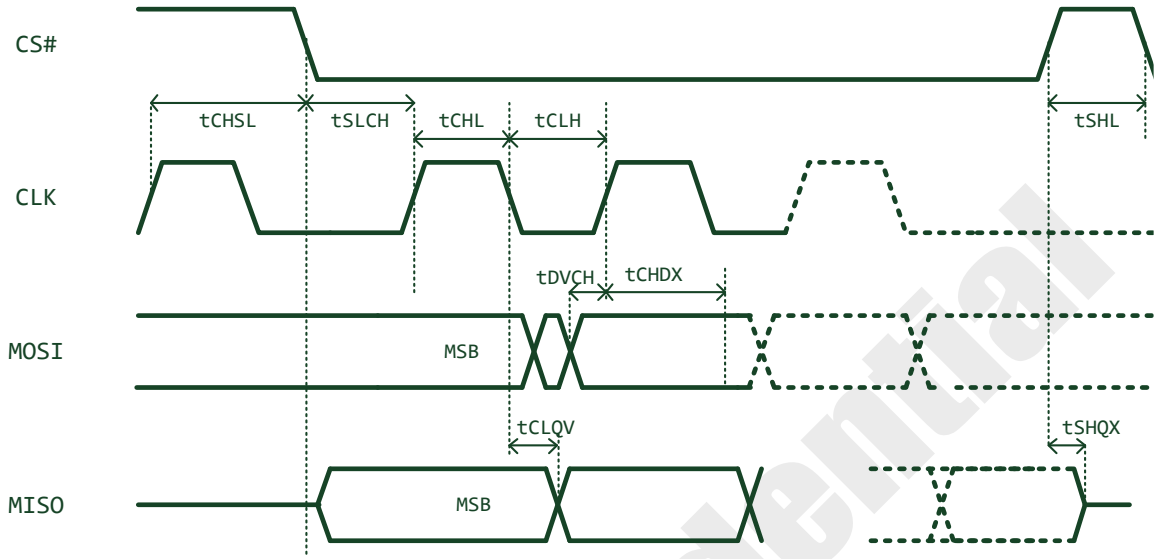


Figure 10: Data SPI Slave Timing

Table 5: Data SPI Slave Timing Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
CS# active hold time	tCHSL	10			ns
CS# active setup time	tSLCH	3			ns
CS# inactive time	tSHL	300			ns
CLK high time	tCHL	12.5			ns
CLK low time	tCLH	12.5			ns
Data in (MISO) setup time	tDVCH	3			ns
Data in (MISO) hold time	tCHDX	3			ns
Data output delay	tCLQV			6.5	ns
Data output disable time	tSHQX			6	ns

4 DC CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings in Table 6 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 6: Absolute Maximum Ratings

Symbol (domain)	Description	Max Rating	Unit
AVDD11_SX	VDD input for analog 1.1V	-0.3 to 1.8	V
AVDD11_RF	VDD input for analog 1.1V	-0.3 to 1.8	V
AVDD33_SX	VDD input for external components I/O control	-0.3 to 3.6	V
AVDD33_PA	VDD input for external components I/O control	-0.3 to 3.6	V
AVDD33_TX	VDD input for external components I/O control	-0.3 to 3.6	V
DVDDIO1	VDD input for GPIO pins	-0.3 to 3.6	V
DVDDIO2/DVDDIO23	VDD input for GPIO pins	-0.3 to 3.6	V
DVDDIO3	VDD input for GPIO pins	-0.3 to 3.6	V
DVDDIO5V	VDD input for GPIO pins	-0.3 to 5.5	V
DVDD08_DIG	VDD output for internal digital circuit	-0.3 to 1.0	V
DVDD11_DIG	VDD input for digital circuit's LDO	-0.3 to 1.4	V
VBAT	VDD input for VBAT	-0.3 to 5.5	V
AVDD33_DCDC	VDD input for DCDC	-0.3 to 3.6	V
AVDD33_RTC	RTC domain power supply	-0.3 to 3.6	V
VREF_IOTADC	ADC power supply	-0.3 to 3.6	V

4.2 ENVIRONMENTAL RATINGS

The environmental ratings are shown in Table 7

Table 7: Environmental Ratings

	Part Number	Value	Units
Operating Temperature(T_A)	SV32WB0xx	-40 to +85	°C
Operating Temperature(T_A)	SV32WB0xx(-H)	-40 to +105	°C

4.3 STORAGE CONDITION

The calculated shelf life in sealed bag is 12 months if stored between 0°C and 40°C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

a) Mounted within 168-hours of factory conditions < 30 **°C** /60%RH
b) Storage humidity needs to maintained at <10% RH
c) Baking is necessary if customer exposes the component to air over 168 hours, baking condition: 125°C / 8hours

4.4 THERMAL CHARACTERISTICS

Table 8: The thermal characteristics of the SV32WB0xx

Thermal characteristics without external heat sink in still air condition

Symbol	Description	Typ.	Unit
T_J	Maximum Junction Temperature (Plastic Package)	125	°C
θ_{JA}	Thermal Resistance θ_{JA} (°C /W) for JEDEC 4L system PCB	37.8	°C/W
θ_{JC}	Thermal Resistance θ_{JC} (°C /W) for JEDEC 4L system PCB	TBD	°C/W
Ψ_{Jt}	Thermal Characterization parameter Ψ_{Jt} (°C /W) for JEDEC 4L system PCB	4.13	°C/W
	Maximum Lead Temperature (Soldering 10s)	260	°C

Notes: * JEDEC 51-7 system FR4 PCB size: 3” x 4.5” (76.2 x 114.3 mm)

* Thermal characteristics without external heat sink in still air condition

4.5 ELECTROSTATIC DISCHARGE SPECIFICATIONS

This is an ESD sensitive product. Observe precaution and handle with care. Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices.

Table 9: ESD Specifications

ESD Mode	Standard	Pin Name	Value	Unit
Human Body Mode (HBM)	JEDEC EIA/JESD22-A114	All pins exclude XO/XI	±3000	V
		XO/XI	±2000	V

JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process

4.6 POWER-ON HOURS(POH)

This information is provided solely for your convenience and does not extend or modify the warranty provided under iComm's standard terms and conditions for iComm semiconductor products.

Table 10: Power-On Hours

OPERATION CONDITION	Part Number	Power-On Hours(POH)(hours)
T_A up to 85°C [a]	SV32WB0xx	87600
T_A up to 105°C [a]	SV32WB0xx(-H)	87600

a. The TX duty cycle (power amplifier ON time) is assumed to be 10% of the device POH. Of the remaining 90% of the time, the device can be in any other state.

4.7 Recommended Operating Conditions and DC Characteristics

Table 11: Recommended Operating Conditions and DC Characteristics

Domain (Symbol)	Description	Min.	Typ.	Max.	Unit
AVDD11_SX	VDD input for analog 1.1V	0.9	1.1	1.3	V
AVDD11_RF	VDD input for analog 1.1V	0.9	1.1	1.3	V
AVDD33_SX	VDD input for external components I/O control	2.1	3.3	3.46	V
AVDD33_PA	VDD input for external components I/O control	2.1	3.3	3.46	V
AVDD33_TX	VDD input for external components I/O control	2.1	3.3	3.46	V
DVDDIO1	VDD input for GPIO pins	1.75	3.3	3.46	V
DVDDIO2/DVDDIO23	VDD input for GPIO pins	1.75	3.3	3.46	V
DVDDIO3	VDD input for GPIO pins	1.75	3.3	3.46	V
DVDDIO5V	VDD input for GPIO pins	1.75	3.3	5.25	V
DVDD08_DIG	VDD output for internal digital circuit		0.8		V
DVDD11_DIG	VDD input for digital circuit's LDO		1.1		V
VBAT with 5v*[a]	VDD input	3.3	5	5.25	V
RVDD33*[a]	VDD output		3.3		V
VBAT/RVDD33 with 0v*[b]	VDD input/VDD output		0		V
AVDD33_DCDC	VDD input for DCDC	2.1	3.3	3.46	V
AVDD33_RTC	RTC domain power supply	2.1	3.3	3.46	V
AVDD33_IOTADC	ADC power supply	1.75	3.3	3.46	V
(V_{IL})	Input Low voltage when VDDIO=3.3V	-0.3		0.8	V
(V_{IH})	Input High voltage when VDDIO=3.3V	2		3.6	V
(V_{T+})	Schmitt trigger low to high threshold voltage when VDDIO=3.3V	1.52	1.63	1.77	V
(V_{T-})	Schmitt trigger high to low threshold voltage when VDDIO=3.3V	1.29	1.41	1.56	V
(V_{OL})	Output low voltage when VDDIO=3.3V			0.4	V
(V_{OH})	Output high voltage when VDDIO=3.3V	2.4			V
(R_{PD})	Input weakly pull-down resistance when VDDIO=3.3V. All GPIO pins have internal weakly pull- down option except that GPIO_5 has internal weakly pull-up option				KΩ
(R_{PU})	Input weakly pull-high resistance when VDDIO=3.3V. All GPIO pins have internal weakly pull- down option except that GPIO_5 has internal weakly pull-up option				KΩ

Domain (Symbol)	Description	Min.	Typ.	Max.	Unit
VIH_nRST	Chip reset release voltage		>1		V
VIL_nRST	Chip reset voltage		<0.1		V
(I_{OL}) – level 1*c	Low level output current @ V_{OL}(max), 8mA setting	5.2	7.52	10.09	mA
	Low level output current @ V_{OL}(max), 12mA setting	10.4	15.03	20.2	mA
(I_{OH}) – level 1*c	High level output current @ V_{OH}(min), 8mA setting	6.8	12.08	18.44	mA
	High level output current @ V_{OH}(min), 12mA setting	12.7	22.64	35.09	mA
(I_{OL}) – level 2*c	Low level output current @ V_{OL}(max), 8mA setting	14.6	21.1	28.27	mA
	Low level output current @ V_{OL}(max), 12mA setting	19.8	28.58	38.4	mA
(I_{OH}) – level 2*c	High level output current @ V_{OH}(min), 8mA setting	17.9	32.03	48.7	mA
	High level output current @ V_{OH}(min), 12mA setting	24.7	42.95	66.8	mA

Note: The total current limitations in GPIO power domain DVDDIO1 and DVDDIO23 are both 51.31mA respectively for QFN32; The total current limitations in GPIO power domain DVDDIO1 and DVDDIO23 are 51.31mA and 70.42mA respectively for QFN40; The total current limitations in GPIO power domain DVDDIO1, DVDDIO2 and DVDDIO3 are 51.31mA, 51.31mA and 35.21mA respectively for QFN60. The definition of the GPIO power domain is in the Table 22: SV32WB0xx Power domains.

*a: In 5v application, VBAT connects to 5v, RVDD33 can provide 3.3v.

*b: In 3.3v application, VBAT connects to 0v, RVDD33 is connected to 0v as well.

*c: Level definition is in the Table 21: SV32WB0xx Package Pin-out

5 FREQUENCY REFERENCES

5.1 CRYSTAL OSCILLATOR SPECIFICATIONS

Table 12: Crystal Oscillator Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency	–	24/26/40 MHz			
Crystal load Capacitance	–	–	10		pF
ESR	–	–	–	70	Ω
Frequency tolerance Initial and over temperature	–	-20	–	20	ppm

5.2 EXTERNAL CLOCK-REQUIREMENTS AND PERFORMANCE

Table 13: External Clock-Requirements and Performance

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency	–	24/26/40 MHz			
OSCIN Input Voltage	AC-couple analog signal	400	–	900	mV_{PP}
Frequency tolerance Initial and over temperature	–	-20	–	20	ppm
Duty Cycle	26MHz clock	40	50	60	%
Phase Noise (802.11b/g)	26MHz clock at 1KHz offset	–	–	–119	dBc/Hz
	26MHz clock at 10KHz offset	–	–	–129	dBc/Hz
	26MHz clock at 100KHz offset	–	–	–134	dBc/Hz
	26MHz clock at 1MHz offset	–	–	–139	dBc/Hz
Phase Noise (802.11n 2.4GHz)	26MHz clock at 1KHz offset	–	–	–125	dBc/Hz
	26MHz clock at 10KHz offset	–	–	–135	dBc/Hz
	26MHz clock at 100KHz offset	–	–	–140	dBc/Hz
	26MHz clock at 1MHz offset	–	–	–145	dBc/Hz

6 ELECTRICAL SPECIFICATIONS

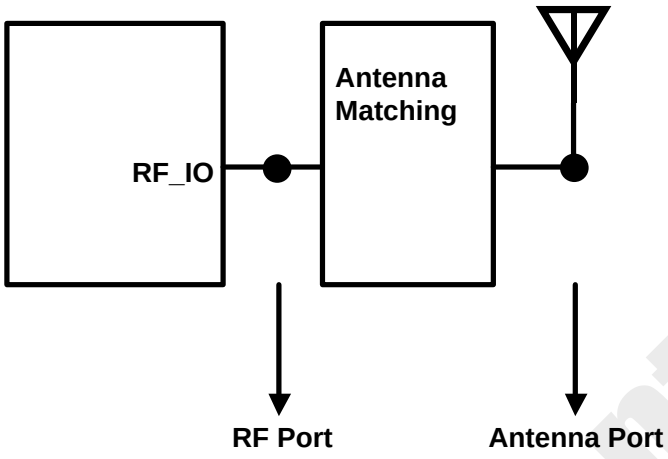


Figure 11: RF Front-End Reference Topology for RF Performance

Note: All specifications are measured at the RF Port unless otherwise specified.

6.1 WLAN RF Performance Specifications

Table 14: 2.4G WLAN RF Performance Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range		2412	-	2484	MHz
Rx Sensitivity (CCK)	CCK, 1 Mbps		-97.5		dBm
	CCK, 2 Mbps		-94.5		dBm
	CCK, 5.5 Mbps		-92.5		dBm
	CCK, 11 Mbps		-89.0		dBm
Rx Sensitivity (OFDM)	OFDM, 6 Mbps		-92.5		dBm
	OFDM, 9 Mbps		-91.5		dBm
	OFDM, 12 Mbps		-89.5		dBm
	OFDM, 18 Mbps		-87.5		dBm
	OFDM, 24 Mbps		-84.5		dBm
	OFDM, 36 Mbps		-81.5		dBm
	OFDM, 48 Mbps		-76.5		dBm
	OFDM, 54 Mbps		-75.5		dBm
Rx Sensitivity (HT20) Mixed mode 800nS GI Non-STBC	HT20, MCS0		-92.0		dBm
	HT20, MCS1		-89.0		dBm
	HT20, MCS2		-87.0		dBm
	HT20, MCS3		-84.0		dBm
	HT20, MCS4		-81.0		dBm
	HT20, MCS5		-76.0		dBm
	HT20, MCS6		-75.0		dBm
	HT20, MCS7		-73.5		dBm
Rx Sensitivity (HT40) Mixed mode 800nS GI Non-STBC	HT40, MCS0		-88.5		dBm
	HT40, MCS1		-85.5		dBm
	HT40, MCS2		-83.5		dBm
	HT40, MCS3		-80.5		dBm
	HT40, MCS4		-77.5		dBm
	HT40, MCS5		-73		dBm
	HT40, MCS6		-71.5		dBm
	HT40, MCS7		-70.5		dBm
Parameter	**Condition/Notes**	**Min.**	**Typ.**	**Max.**	**Unit**
RX Adjacent Channel Rejection (CCK)	1 Mbps		41		dB
	11 Mbps		41		dB
RX Adjacent Channel Rejection (OFDM)	6 Mbps		39		dB
	54 Mbps		23		dB
RX Adjacent Channel Rejection (HT20)	MCS0		38		dB
	MCS7		21		dB
RX Adjacent Channel Rejection (HT40)	MCS0		30		dB
	MCS7		11		dB

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
TX Output Power (with PADPD)	CCK, 1-11 Mbps		19		dBm
	OFDM, 54 Mbps		15		dBm
	HT20, MCS7		15		dBm
	HT40,MCS7		15		dBm

6.2 BLUETOOTH RF PERFORMANCE SPECIFICATIONS

Table 15: Bluetooth RF Performance Specifications

TX Characteristic	Min.	Typ.	Max.	Unit
Frequency Range	2402	-	2480	MHz
Output power	0	6	10	dBm
Carrier Frequency Offset and Drift				
Frequency Offset	-150		150	KHz
Frequency Drift	-50		50	KHz
Max Drift Rate	-20		20	KHz/50us
Modulation Characteristic				
△f1avg	225		275	KHz
△f2max	185			KHz
△f1avg/△f2avg	0.8	0.94		
In-band Spurious Emission				
±2M Offset			-20	dBm
＞±3MHz offset			-30	dBm

RX Characteristic	Min.	Typ.	Max.	Unit
Frequency Range	2402	-	2480	MHz
Receiver Sensitivity		-94		dBm
C/I Co-channel		6.5	21	dB
C/I 1MHz		4	15	dB
C/I 2MHz		-21	-17	dB
C/I ≥3MHz		-30	-27	dB
C/I Image channel		NA		dB
C/I Image 1MHz		NA		dB
Inter-modulation	-50	-35		dBm
Out-of-band blocking				
30MHz to 2000MHz	-30			dBm
2001MHz to 2339MHz	-35			dBm
2501MHz to 3000MHz	-35			dBm
3001MHz to 12.75GHz	-30			dBm

7 System Power Consumption

Table 16: Power Consumption at DCDC mode (DCDC buck convertor is enable)

WLAN Operational Modes	Typ.[c]	Unit
OFF[a]	1.5	uA
Rx, CCK, 1 Mbps[e]	33	mA
Rx, OFDM, 54 Mbps[e]	33	mA
Rx, HT20, MCS7[e]	33	mA
Rx, HT40, MCS7[e]	33	mA
Tx, CCK, 1 Mbps@19dBm[d]	212	mA
Tx, OFDM, 54 Mbps@15dBm[d]	182	mA
Tx, HT20, MCS7@15dBm[d]	183	mA
Tx, HT40, MCS7@15dBm[d]	183	mA
Power-saving(MCU_off)[b] , DTIM1	0.43	mA
Power-saving(MCU_off)[b] , DTIM3	0.21	mA
Power-saving(MCU_off)[b] , DTIM3 with SV32WB0xL	0.150	mA

Table 17: Power Consumption at LDO mode (DCDC buck convertor is disable)

WLAN Operational Modes	Typ.[c]	Unit
OFF[a]	1.5	uA
Rx, CCK, 1 Mbps[e]	80	mA
Rx, OFDM, 54 Mbps[e]	80	mA
Rx, HT20, MCS7[e]	80	mA
Rx, HT40, MCS7[e]	80	mA
Tx, CCK, 1 Mbps@19dBm[d]	243	mA
Tx, OFDM, 54 Mbps@15dBm[d]	214	mA
Tx, HT20, MCS7@15dBm[d]	215	mA
Tx, HT40, MCS7@15dBm[d]	215	mA
Power-saving(MCU_off)[b] , DTIM1	1.20	mA
Power-saving(MCU_off)[b] , DTIM3	0.45	mA

a. OFF mode test condition: VBAT=GND, RDVDD=GND, VIO=3.3V, LDO_EN=0V (excluding Flash/PSRAM).
b. Intra-beacon Sleep when MCU is turn off.
c. Conditions: VBAT=GND, RVD33=GND, VDDIO=3.3V
d. When the CPU CLK is 160MHz, the Tx current increases 10mA, when the CPU CLK is 320MHz, the Tx current increases 20mA
e. When the CPU CLK is 160MHz, the Rx current increases 6mA, when the CPU CLK is 320MHz, the Rx current increases 12mA

8 PIN DESCRIPTIONS

8.1 PIN LAYOUT

This section contains a listing of the signal descriptions (see Figure 12 for the SV32WB01x package pin-out)

Figure 12: SV32WB01x Pin Assignment –QFN32 (top view)

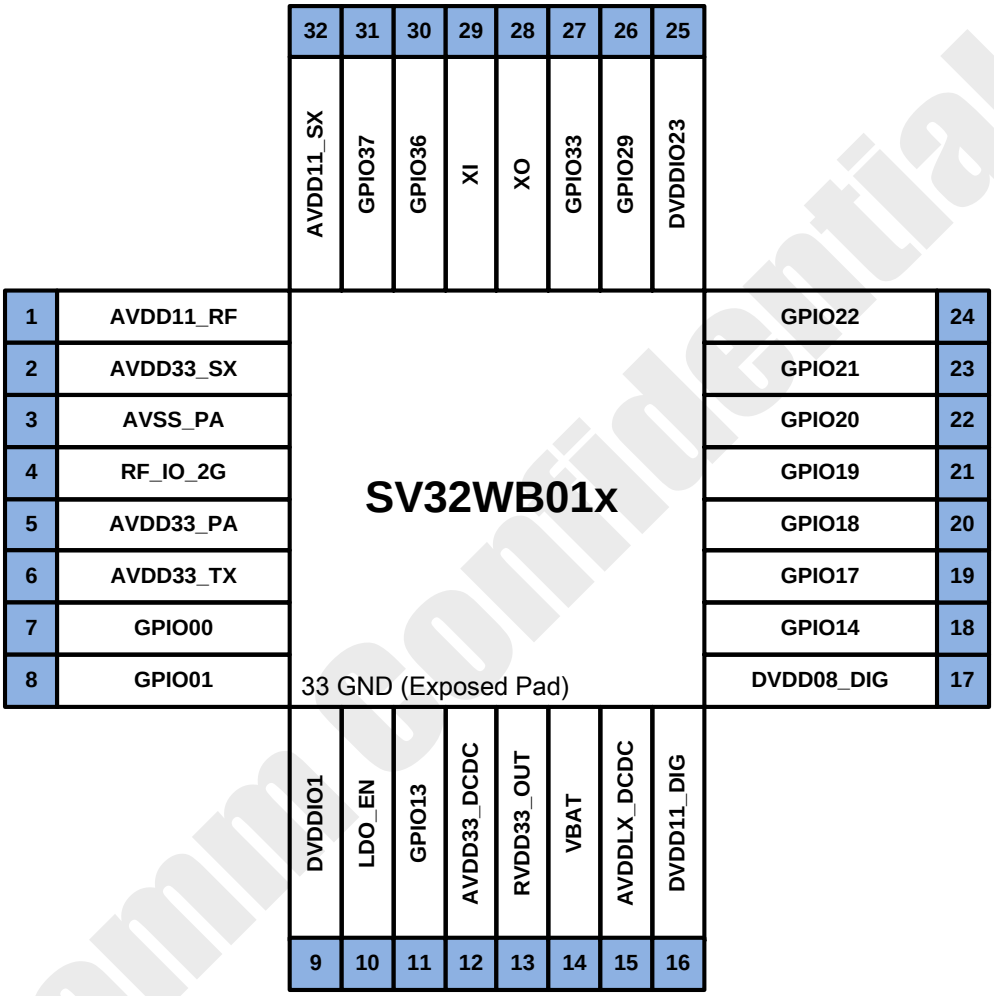


Table 18: SV32WB01x Pin coordination

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	AVDD11_RF	2	AVDD33_SX	3	AVSS_PA	4	RF_IO_2G
5	AVDD33_PA	6	AVDD33_TX	7	GPIO00	8	GPIO01
9	DVDDIO1	10	LDO_EN	11	GPIO13	12	AVDD33_DCDC
13	RVDD33_OUT	14	VBAT	15	AVDDLX_DCDC	16	DVDD11_DIG
17	DVDD08_DIG	18	GPIO14	19	GPIO17	20	GPIO18
21	GPIO19	22	GPIO20	23	GPIO21	24	GPIO22
25	DVDDIO23	26	GPIO29	27	GPIO33	28	XO
29	XI	30	GPIO36	31	GPIO37	32	AVDD11_SX

This section contains a listing of the signal descriptions (see Figure 13 for the SV32WB05/SV32WB07 package pin-out)

Figure 13: SV32WB05/SV32WB07 Pin Assignment –QFN40 (top view)

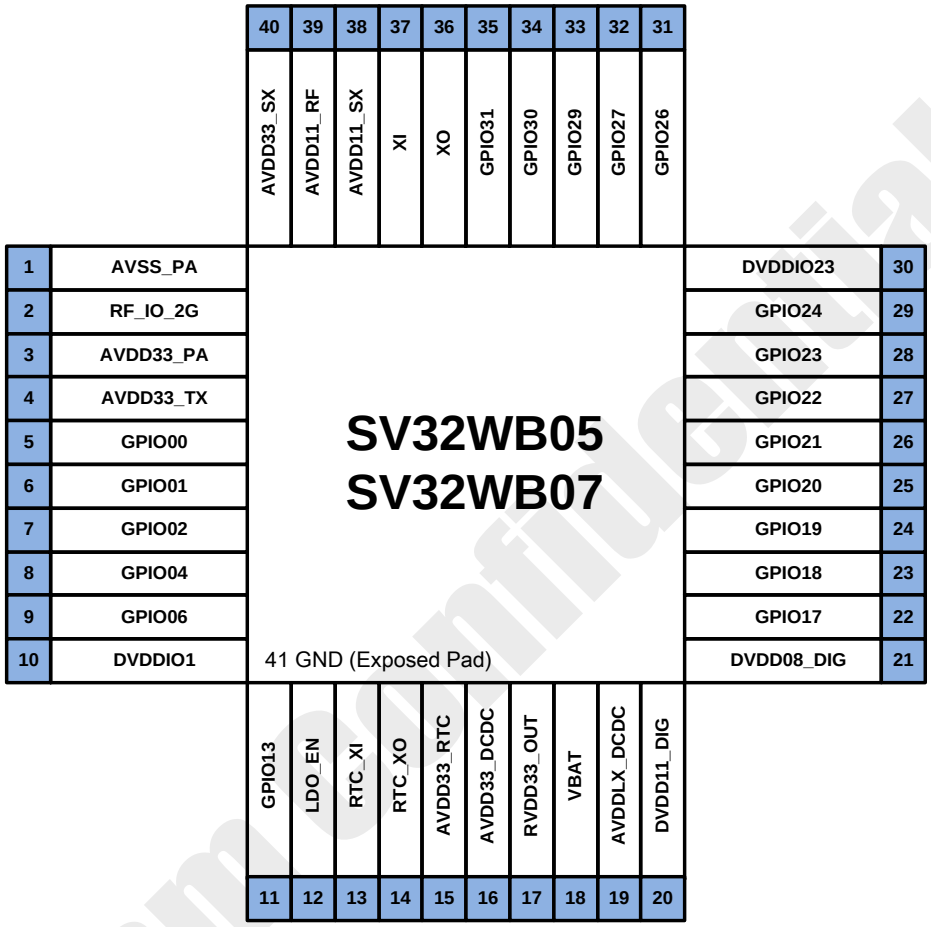


Table 19: SV32WB05/SV32WB07 Pin coordination

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	AVSS_PA	2	RF_IO_2G	3	AVDD33_PA	4	AVDD33_TX
5	GPIO00	6	GPIO01	7	GPIO02	8	GPIO04
9	GPIO06	10	DVDDIO1	11	GPIO13	12	LDO_EN
13	RTC_XI	14	RTC_XO	15	AVDD33_RTC	16	AVDD33_DCDC
17	RVDD33_OUT	18	VBAT	19	AVDDLX_DCDC	20	DVDD11_DIG
21	DVDD08_DIG	22	GPIO17	23	GPIO18	24	GPIO19
25	GPIO20	26	GPIO21	27	GPIO22	28	GPIO23
29	GPIO24	30	DVDDIO23	31	GPIO26	32	GPIO27
33	GPIO29	34	GPIO30	35	GPIO31	36	XO
37	XI	38	AVDD11_SX	39	AVDD11_RF	40	AVDD33_SX

This section contains a listing of the signal descriptions (see Figure 14 for the SV32WB06 package pin-out)

Figure 14: SV32WB06 Pin Assignment –QFN60 (top view)

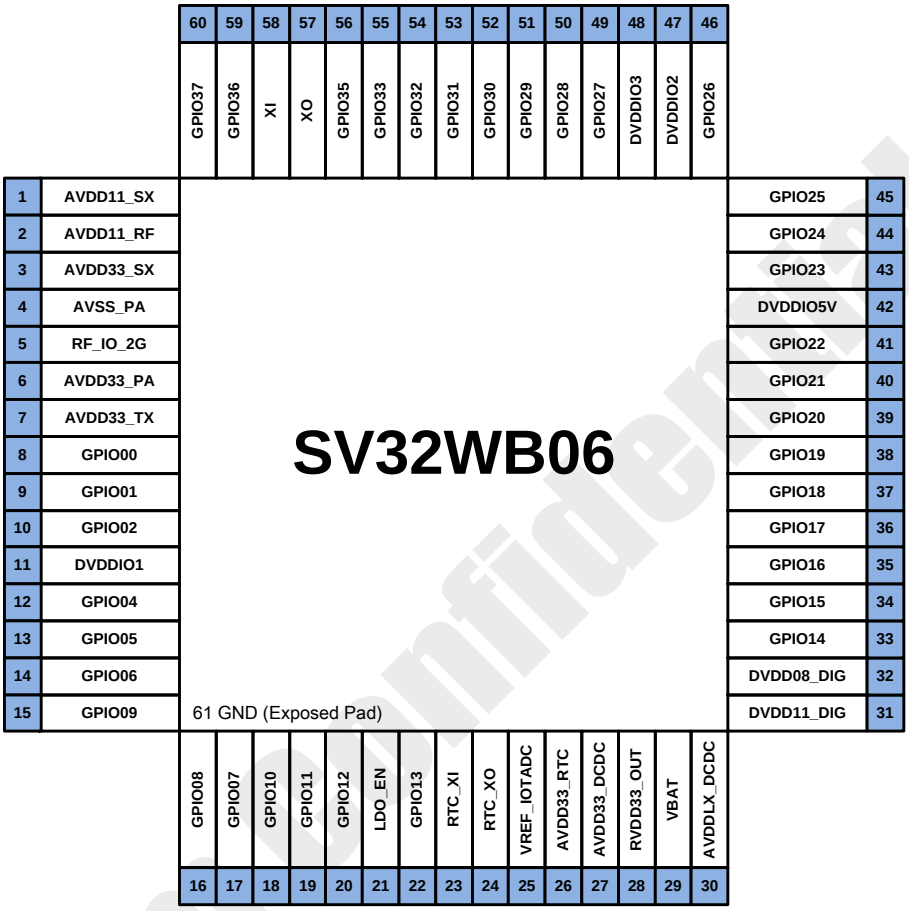


Table 20: SV32WB06 Pin coordination

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	AVDD11_SX	2	AVDD11_RF	3	AVDD33_SX	4	AVSS_PA
5	RF_IO_2G	6	AVDD33_PA	7	AVDD33_TX	8	GPIO00
9	GPIO01	10	GPIO02	11	DVDDIO1	12	GPIO04
13	GPIO05	14	GPIO06	15	GPIO09	16	GPIO08
17	GPIO07	18	GPIO10	19	GPIO11	20	GPIO12
21	LDO_EN	22	GPIO13	23	RTC_XI	24	RTC_XO
25	VREF_IOTADC	26	AVDD33_RTC	27	AVDD33_DCDC	28	RVDD33_OUT
29	VBAT	30	AVDDLX_DCDC	31	DVDD11_DIG	32	DVDD08_DIG
33	GPIO14	34	GPIO15	35	GPIO16	36	GPIO17
37	GPIO18	38	GPIO19	39	GPIO20	40	GPIO21
41	GPIO22	42	DVDDIO5V	43	GPIO23	44	GPIO24
45	GPIO25	46	GPIO26	47	DVDDIO2	48	DVDDIO3
49	GPIO27	50	GPIO28	51	GPIO29	52	GPIO30
53	GPIO31	54	GPIO32	55	GPIO33	56	GPIO35

57	XO	58	XI	59	GPIO36	60	GPIO37

8.2 PIN DESCRIPTION

Table 21: SV32WB0xx Package Pin-out

Pin Name	QFN32	QFN40	QFN60	Type*	Description	Output current level
General purpose I/O						
GPIO00	7	5	8	I/O	General Purpose I/O Pins	level1
GPIO01	8	6	9	I/O	General Purpose I/O Pins	level1
GPIO02		7	10	I/O	General Purpose I/O Pins	level1
GPIO04		8	12	I/O	General Purpose I/O Pins	level1
GPIO05			13	I/O	General Purpose I/O Pins	level1
GPIO06		9	14	I/O	General Purpose I/O Pins	level2
GPIO07			17	I/O	General Purpose I/O Pins	level2
GPIO08			16	I/O	General Purpose I/O Pins	level2
GPIO09			15	I/O	General Purpose I/O Pins	level2
GPIO10			18	I/O	General Purpose I/O Pins	level2
GPIO11			19	I/O	General Purpose I/O Pins	level2
GPIO12			20	I/O	Purpose I/O Pins	level2
GPIO13	11	11	22	I/O	Strapping Purpose I/O Pins	level1
GPIO14	18		33	I/O	General Purpose I/O Pins	level1
GPIO15			34	I/O	General Purpose I/O Pins	level1
GPIO16			35	I/O	General Purpose I/O Pins	level1
GPIO17	19	22	36	I/O	General Purpose I/O Pins	level2
GPIO18	20	23	37	I/O	General Purpose I/O Pins	level2
GPIO19	21	24	38	I/O	General Purpose I/O Pins	level2
GPIO20	22	25	39	I/O	General Purpose I/O Pins	level2
GPIO21	23	26	40	I/O	General Purpose I/O Pins	level2
GPIO22	24	27	41	I/O	General Purpose I/O Pins	level2
GPIO23		28	43	I/O	General Purpose I/O Pins	level2
GPIO24		29	44	I/O	General Purpose I/O Pins	level2
GPIO25			45	I/O	General Purpose I/O Pins	level1
GPIO26		31	46	I/O	General Purpose I/O Pins	level1
GPIO27		32	49	I/O	General Purpose I/O Pins	level1
GPIO28			50	I/O	Strapping Purpose I/O Pins	level1
GPIO29	26	33	51	I/O	General Purpose I/O Pins	level1
GPIO30		34	52	I/O	General Purpose I/O Pins	level1
GPIO31		35	53	I/O	General Purpose I/O Pins	level1
GPIO32			54	I/O	General Purpose I/O Pins	level1
GPIO33	27		55	I/O	General Purpose I/O Pins	level1
GPIO35			56	I/O	General Purpose I/O Pins	level1

GPIO36	30		59	I/O	General Purpose I/O Pins	level1
GPIO37	31		60	I/O	General Purpose I/O Pins	level1

Pin Name	QFN32	QFN40	QFN60	Type*	Description
IO Power					
DVDDIO1	9	10	11	P	VIO input
DVDDIO5V			42	P	VIO input
DVDDIO2/DVDDIO23	25	30	47	P	VIO input
DVDDIO3			48	P	VIO input
Reset and Clocks					
LDO_EN	10	12	21	I	Reset signal to power down IC
XO	28	36	57	O	Output of crystal clock reference
XI	29	37	58	I	Input of crystal clock reference
Real-time clock					
RTC_XI		13	23	I	Output of 32K clock reference
RTC_XO		14	24	O	Input of 32K clock reference
AVDD33_RTC		15	26	P	RTC 3.3v input
PMU/BUCK					
VREF_IOTADC			25	P	ADC reference Voltage input
AVDD33_DCDC	12	16	27	P	analog 3.3V input for DCDC
RVDD33_OUT	13	17	28	P	Internal LDO output
VBAT	14	18	29	P	Power Supply
AVDDLX_DCDC	15	19	30	P	DCDC buck regulator: output to inductor
DVDD11_DIG	16	20	31	P	DCDC 1.1V output
DVDD08_DIG	17	21	32	P	Digital 0.8V input
WiFi radio					
AVDD11_SX	32	38	1	P	analog 1.1V input
AVDD11_RF	1	39	2	P	analog 1.1V input
AVDD33_SX	2	40	3	P	analog 3.3V input
AVSS_PA	3	1	4	G	Ground
RF_IO_2G	4	2	5	I/O	2.4 GHz RF input & output port
AVDD33_PA	5	3	6	P	analog 3.3V input
AVDD33_TX	6	4	7	P	analog 3.3V input

* I=Input; O=Output; G=Ground; P=Power

Table 22: SV32WB0xx Power domains

Power Domain	QFN32	QFN40	QFN60
DVDDIO1	GPIO00,01,13	GPIO00,01,02,04,06,13	GPIO00,01,02,04,05,06,07, 08,09,10,11,12,13
DVDDIO2			GPIO14,15,16,17,18,19, 20,21,22,25,26
DVDDIO23	GPIO14,17,18,19,20,21,22, 29,33,36,37	GPIO17,18,19,20,21,22,23, 24,26,27,29,30,31	
DVDDIO5V			GPIO23,24
DVDDIO3			GPIO27,28,29,30,31,32,33, 35,36,37

8.3 Mode Selection

Table 23: Mode Selection table

strapping truth table		
GPIO	**Interface mode**	**Description**
GPIO[28]*[a]		
0	IOT	SPI flash w/I in-place execution
1	Reserved	Reserved(default)
GPIO[13]		
0	FlashBoot	Boot from flash (default)
1	IAP*[b]	IAP command accept

*[a] No external pull-down resistor is required because internal pull-down for SV32WB01x/SV32WB05/SV32WB07

*[b] Use GPIO00/GPIO01 as UART Rx/Tx to program the flash for SV32WB01x /SV32WB06; use GPIO30/31 as UART Rx/Tx to program the flash for SV32WB05/SV32WB07

8.4 User Define I/O Function Selection For IOT

After bootstrap, the SV32WB0xx also provides a pad multiplex switching from the bootstrap function to selected I/O function by register signals. There is a condition to leave bootstrap function. That is switching to GPIO first then switching to select I/O function. The Table 24/Table 25/Table 26/Table 27 show the all I/O functions for each PAD.

Table 24: Pinmux for SV32WB01x

Name	Boot Strapping ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
GPIO00	AICE_TMSC	ADC0	BT_SW	UART0_RXD				GPIO00
GPIO01	AICE_TCKC	ADC1	WIFI_TX_SW	UART0_TXD				GPIO01
GPIO13	GPIO13							GPIO13
GPIO14	GPIO14			PDMTX0_DOUT0				GPIO14
GPIO17	GPIO17	SD_DATA2	UART2_NCTS					GPIO17
GPIO18	GPIO18	SD_DATA3		DATASPISLAVE_CSN	SPISLV1_CSN	SPIMAS1_CSN		GPIO18
GPIO19	GPIO19	SD_CMD		DATASPISLAVE_MOSI	SPISLV1_MOSI	SPIMAS1_MOSI		GPIO19
GPIO20	GPIO20	SD_CLK		DATASPISLAVE_SCLK	SPISLV1_MISO	SPIMAS1_MISO		GPIO20
GPIO21	GPIO21	SD_DATA0		DATASPISLAVE_MISO	SPISLV1_SCLK	SPIMAS1_SCLK		GPIO21
GPIO22	GPIO22	SD_DATA1	UART2_NRTS					GPIO22
GPIO29	GPIO29	ADC3			UART1_RXD			GPIO29
GPIO33	GPIO33				UART1_TXD	WIFI_TX		GPIO33
GPIO36	GPIO36	ADC6	I2C0_SCL	UART2_RXD		BT_IN_PROCESS	BT_SW	GPIO36
GPIO37	GPIO37	ADC7	I2C0_SDA	UART2_TXD		BT_PTI3	WIFI_TX_SW	GPIO37

Table 25: Pinmux for SV32WB05/SV32WB07

Name	Boot Strapping ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
GPIO00	AICE_TMSC	ADC0		UART0_RXD		SPIMAS0_MOSI		GPIO00
GPIO01	AICE_TCKC	ADC1		UART0_TXD		SPIMAS0_MISO		GPIO01
GPIO02	GPIO02	ADC2				SPIMAS0_SCLK		GPIO02
GPIO04	GPIO04	I2C0_SCL						GPIO04
GPIO06	GPIO06	I2C0_SDA						GPIO06
GPIO13	GPIO13							GPIO13
GPIO17	GPIO17	SD_DATA2	UART2_NCTS					GPIO17
GPIO18	GPIO18	SD_DATA3		DATASPISLAVE_CSN	SPISLV1_CSN	SPIMAS1_CSN		GPIO18
GPIO19	GPIO19	SD_CMD		DATASPISLAVE_MOSI	SPISLV1_MOSI	SPIMAS1_MOSI		GPIO19
GPIO20	GPIO20	SD_CLK		DATASPISLAVE_SCLK	SPISLV1_MISO	SPIMAS1_MISO		GPIO20
GPIO21	GPIO21	SD_DATA0		DATASPISLAVE_MISO	SPISLV1_SCLK	SPIMAS1_SCLK		GPIO21
GPIO22	GPIO22	SD_DATA1	UART2_NRTS		I2S0_MCLK			GPIO22
GPIO23	GPIO23		UART2_TXD	I2C1_SCL				GPIO23
GPIO24	GPIO24		UART2_RXD	I2C1_SDA				GPIO24
GPIO26	GPIO26			I2S0_MCLK	UART2_RXD			GPIO26
GPIO27	GPIO27		UART1_NCTS	PDMRX0_CLK		I2S1_WS		GPIO27
GPIO29	GPIO29	ADC3	UART1_NRTS	PDMRX0_DIN	UART1_RXD	I2S1_SDI		GPIO29
GPIO30	GPIO30	ADC4	UART1_RXD	PDMRX1_CLK	PDMTX0_DOUT0	I2S1_SDO		GPIO30
GPIO31	GPIO31	ADC5	UART1_TXD	PDMRX1_DIN	PDMTX0_DOUT1	I2S1_SCK		GPIO31

Table 26: PinMux for SV32WB06

Name	Boot Strapping ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
GPIO00	AICE_TMSC	ADC0	BT_SW	UART0_RXD	SPISLV0_MOSI	SPIMAS0_MOSI		GPIO00
GPIO01	AICE_TCKC	ADC1	WIFI_TX_SW	UART0_TXD	SPISLV0_MISO	SPIMAS0_MISO		GPIO01
GPIO02	GPIO02	ADC2			SPISLV0_SCLK	SPIMAS0_SCLK		GPIO02
GPIO04	GPIO04	I2C0_SCL						GPIO04
GPIO05	GPIO05				SPIMAS0_CSN	SPISLV0_CSN		GPIO05
GPIO06	GPIO06	I2C0_SDA	PSRAM_SPI_CSN					GPIO06
GPIO07		FLASH_SPI_HOLD						GPIO07
GPIO08		FLASH_SPI_SCLK						GPIO08
GPIO09		FLASH_SPI_MOSI						GPIO09
GPIO10		FLASH_SPI_CSN						GPIO10
GPIO11		FLASH_SPI_MISO						GPIO11
GPIO12		FLASH_SPI_WPN						GPIO12
GPIO13	GPIO13							GPIO13
GPIO14	GPIO14			PDMTX0_DOUT0	PDMRX0_CLK	I2S0_WS		GPIO14
GPIO15	GPIO15			PDMTX0_DOUT1	PDMRX0_DIN	I2S0_SDI		GPIO15
GPIO16	GPIO16				PDMRX1_CLK	I2S0_SDO		GPIO16
GPIO17	GPIO17	SD_DATA2	UART2_NCTS		PDMRX1_DIN	I2S0_SCK		GPIO17
GPIO18	GPIO18	SD_DATA3		DATASPISLAVE_CSN	SPISLV1_CSN	SPIMAS1_CSN		GPIO18
GPIO19	GPIO19	SD_CMD		DATASPISLAVE_MOSI	SPISLV1_MOSI	SPIMAS1_MOSI		GPIO19
GPIO20	GPIO20	SD_CLK		DATASPISLAVE_SCLK	SPISLV1_MISO	SPIMAS1_MISO		GPIO20
GPIO21	GPIO21	SD_DATA0		DATASPISLAVE_MISO	SPISLV1_SCLK	SPIMAS1_SCLK		GPIO21
GPIO22	GPIO22	SD_DATA1	UART2_NRTS		I2S0_MCLK			GPIO22
GPIO23	GPIO23		UART2_TXD	I2C1_SCL				GPIO23
GPIO24	GPIO24		UART2_RXD	I2C1_SDA				GPIO24
GPIO25	GPIO25	WIFI_TX	RTC_RC32K_EXT		UART2_TXD			GPIO25
GPIO26	GPIO26	BT_IN_PROCESS		I2S0_MCLK	UART2_RXD	SPIMAS2_CSN		GPIO26
GPIO27	GPIO27		UART1_NCTS	PDMRX0_CLK		I2S1_WS		GPIO27
GPIO28	GPIO28					I2S0_MCLK		GPIO28
GPIO29	GPIO29	ADC3	UART1_NRTS	PDMRX0_DIN	UART1_RXD	I2S1_SDI		GPIO29
GPIO30	GPIO30	ADC4	UART1_RXD	PDMRX1_CLK	PDMTX0_DOUT0	I2S1_SDO		GPIO30
GPIO31	GPIO31	ADC5	UART1_TXD	PDMRX1_DIN	PDMTX0_DOUT1	I2S1_SCK		GPIO31
GPIO32	GPIO32	BT_PTI3		SPIMAS2_SCLK				GPIO32
GPIO33	GPIO33			SPIMAS2_MOSI	UART1_TXD	WIFI_TX		GPIO33
GPIO35	GPIO35			SPIMAS2_MISO				GPIO35
GPIO36	GPIO36	ADC6	I2C0_SCL	UART2_RXD	SPIMAS2_CSN	BT_IN_PROCESS	BT_SW	GPIO36
GPIO37	GPIO37	ADC7	I2C0_SDA	UART2_TXD		BT_PTI3	WIFI_TX_SW	GPIO37

Table 27: Pinmux Description for SV32WB0xx

GPIO Name	Pin No. QFN32	Pin No. QFN40	Pin No. QFN60	Alternate Functions		
				OEN	REN	Function
GPIO00	7	5	8	I	F	ADC0
				O	F	BT_SW
				I	F	UART0_RXD
				I	F	SPISLV0_MOSI
				O	PU	SPIMAS0_MOSI
				I/O	F	GPIO00
GPIO01	8	6	9	I	F	ADC1
				O	F	WIFI_TX_SW
				O	F	UART0_TXD
				O	F	SPISLV0_MISO
				I	PU	SPIMAS0_MISO
				I/O	F	GPIO01
GPIO02		7	10	I	F	ADC2
				CI	F	SPISLV0_SCLK
				CO	PD	SPIMAS0_SCLK
				I/O	F	GPIO02
GPIO04		8	12	CI/O	PU	I2C0_SCL
				I/O	F	GPIO04
GPIO05			13	O	PU	SPIMAS0_CSN
				I	F	SPISLV0_CSN
				I/O	F	GPIO05
GPIO06		9	14	I/O	PU	I2C0_SDA
				O	PU	PSRAM_SPI_CSN
				I/O	F	GPIO06
GPIO07			17	I/O	PU	FLASH_SPI_HOLD
				I/O	F	GPIO07
GPIO08			16	O	PD	FLASH_SPI_SCLK
				I/O	F	GPIO08
GPIO09			15	I/O	PD	FLASH_SPI_MOSI
				I/O	F	GPIO09
GPIO10			18	O	PU	FLASH_SPI_CSN
				I/O	F	GPIO10
GPIO11			19	I/O	PD	FLASH_SPI_MISO
				I/O	F	GPIO11
GPIO12			20	I/O	PU	FLASH_SPI_WPN
				I/O	F	GPIO12
GPIO13	11	11	22	I/O	F	GPIO13
GPIO14	18		33	O	F	PDMTX0_DOUT0
				O	F	PDMRX0_CLK
				I/O	F	I2S0_WS
				I/O	F	GPIO14
GPIO15			34	O	F	PDMTX0_DOUT1
				I	F	PDMRX0_DIN
				I	F	I2S0_SDI
				I/O	F	GPIO15
GPIO16			35	O	F	PDMRX1_CLK
				O	F	I2S0_SDO
				I/O	F	GPIO16

GPIO Name	Pin No. QFN32	Pin No. QFN40	Pin No. QFN60	Alternate Functions		
				OEN	REN	Function
GPIO17	19	22	36	I/O	F	SD_DATA2
				I	F	UART2_NCTS
				I	F	PDMRX1_DIN
				CI/O	F	I2S0_SCK
				I/O	F	GPIO17
GPIO18	20	23	37	I/O	F	SD_DATA3
				I	F	DATASPISLAVE_CSN
				I	F	SPISLV1_CSN
				O	PU	SPIMAS1_CSN
				I/O	F	GPIO18
GPIO19	21	24	38	I/O	F	SD_CMD
				I	F	DATASPISLAVE_MOSI
				I	F	SPISLV1_MOSI
				O	PU	SPIMAS1_MOSI
				I/O	F	GPIO19
GPIO20	22	25	39	CI	F	SD_CLK
				CI	F	DATASPISLAVE_SCLK
				O	F	SPISLV1_MISO
				I	PU	SPIMAS1_MISO
				I/O	F	GPIO20
GPIO21	23	26	40	I/O	F	SD_DATA0
				O	F	DATASPISLAVE_MISO
				CI	F	SPISLV1_SCLK
				CO	PD	SPIMAS1_SCLK
				I/O	F	GPIO21
GPIO22	24	27	41	I/O	F	SD_DATA1
				O	F	UART2_NRTS
				CO	F	I2S0_MCLK
				I/O	F	GPIO22
GPIO23		28	43	O	PU	UART2_TXD
				CI/O	PU	I2C1_SCL
				I/O	F	GPIO23
GPIO24		29	44	I	F	UART2_RXD
				I/O	PU	I2C1_SDA
				I/O	F	GPIO24
GPIO25			45	O	F	WIFI_TX
				CI	F	RTC_RC32K_EXT
				O	PU	UART2_TXD
				I/O	F	GPIO25
GPIO26		31	46	I	F	BT_IN_PROCESS
				CO	F	I2S0_MCLK
				I	F	UART2_RXD
				O	PU	SPIMAS2_CSN
				I/O	F	GPIO26
GPIO27		32	49	I	F	UART1_NCTS
				O	F	PDMRX0_CLK
				I/O	F	I2S1_WS
				I/O	F	GPIO27
GPIO28			50	CO	F	I2S0_MCLK
				I/O	F	GPIO28

GPIO Name	Pin No. QFN32	Pin No. QFN40	Pin No. QFN60	Alternate Functions OEN	REN	Function
GPIO29	26	33	51	I	F	ADC3
				O	F	UART1_NRTS
				I	F	PDMRX0_DIN
				I	F	UART1_RXD
				I	F	I2S1_SDI
				I/O	F	GPIO29
GPIO30		34	52	I	F	ADC4
				I	F	UART1_RXD
				O	F	PDMRX1_CLK
				O	F	PDMTX0_DOUT0
				O	F	I2S1_SDO
				I/O	F	GPIO30
GPIO31		35	53	I	F	ADC5
				O	PU	UART1_TXD
				I	F	PDMRX1_DIN
				O	F	PDMTX0_DOUT1
				CI/O	F	I2S1_SCK
				I/O	F	GPIO31
GPIO32			54	I	F	BT_PTI3
				CO	PD	SPIMAS2_SCLK
				I/O	F	GPIO32
GPIO33	27		55	O	PU	SPIMAS2_MOSI
				O	PU	UART1_TXD
				O	F	WIFI_TX
				I/O	F	GPIO33
GPIO35			56	I	PU	SPIMAS2_MISO
				I/O	F	GPIO35
GPIO36	30		59	I	F	ADC6
				CI/O	PU	I2C0_SCL
				I	F	UART2_RXD
				O	PU	SPIMAS2_CSN
				I	F	BT_IN_PROCESS
				O	F	BT_SW
				I/O	F	GPIO36
GPIO37	31		60	I	F	ADC7
				I/O	PU	I2C0_SDA
				O	PU	UART2_TXD
				I	F	BT_PTI3
				O	F	WIFI_TX_SW
				I/O	F	GPIO37

8.5 IOT ADC

SV32WB0xx provides an ADC named IOT_ADC for sensing external voltage. It is an inverse binary thermal code design, the more the voltage, the less the data read.

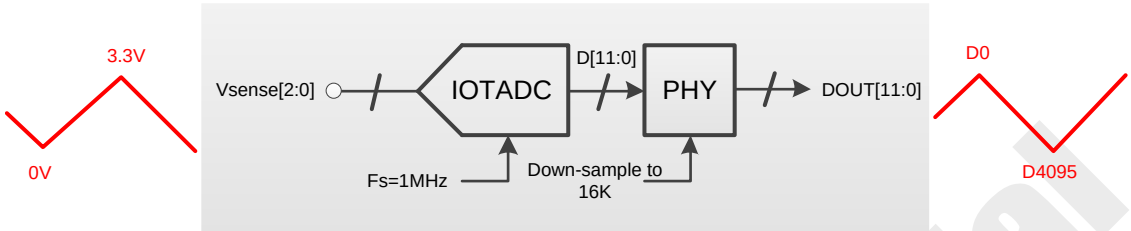


Figure 15: ADC Block diagram

Table 28: IOT ADC Pin Location

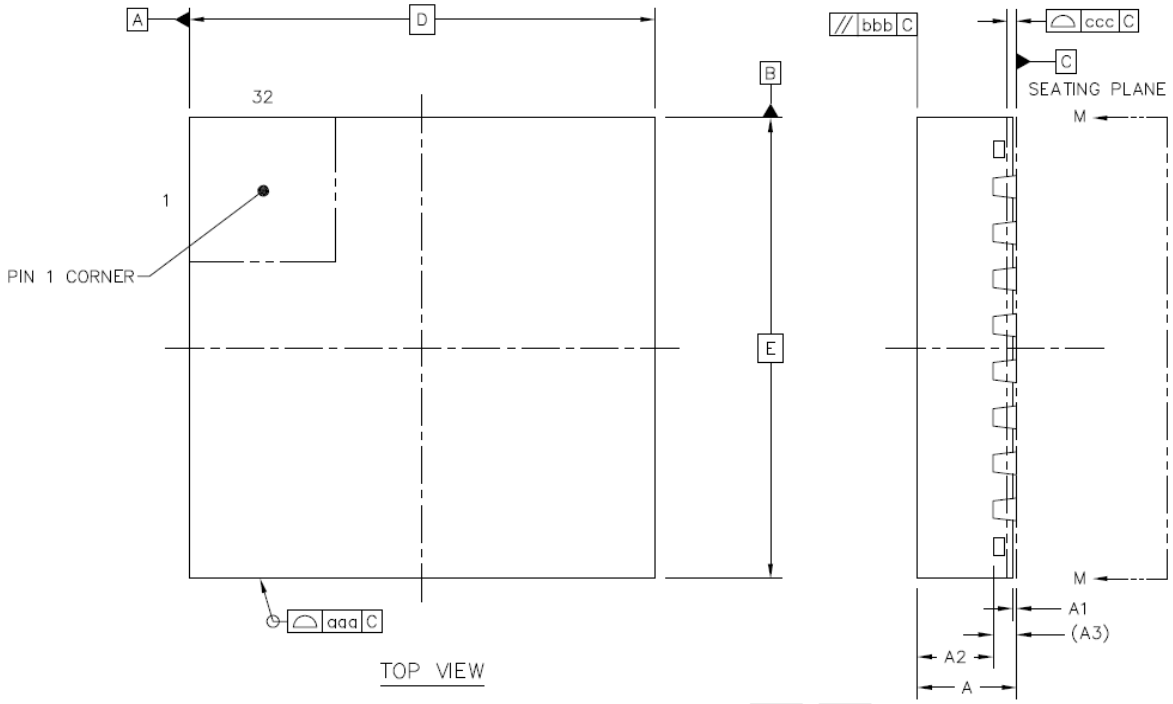
IOT ADC inputs	SV32WB01x (QFN32)		SV32WB05/SV32WB07 (QFN40)		SV32WB06 (QFN60)	
	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
ADC0	7	GPIO00	5	GPIO00	8	GPIO00
ADC1	8	GPIO01	6	GPIO01	9	GPIO01
ADC2			7	GPIO02	10	GPIO02
ADC3	26	GPIO29	33	GPIO29	51	GPIO29
ADC4			34	GPIO30	52	GPIO30
ADC5			35	GPIO31	53	GPIO31
ADC6	30	GPIO36			59	GPIO36
ADC7	31	GPIO37			60	GPIO37

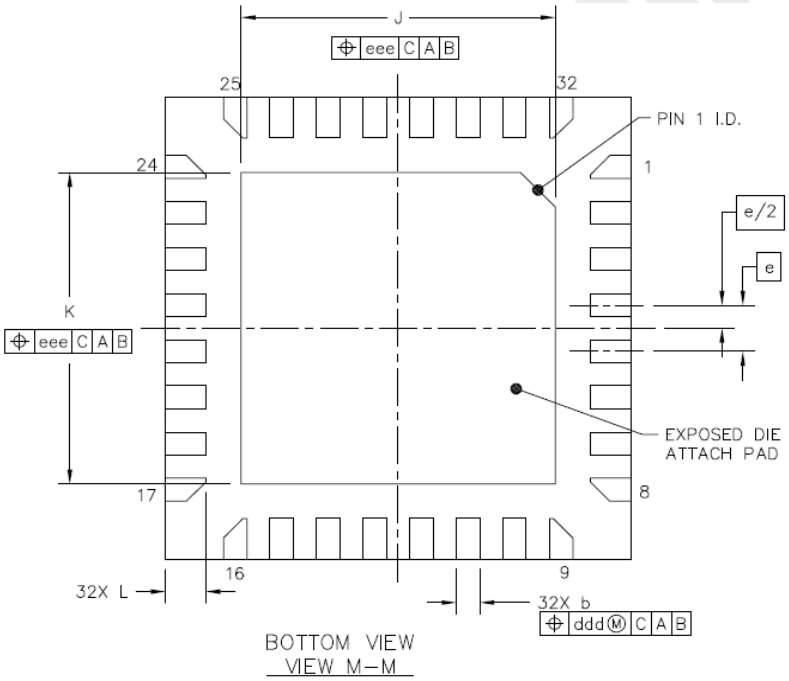
Table 29: IOT ADC Specifications

Parameter	Description	Condition/Notes	Min	Typ.	Max	Unit
Nbits	Number of bits			12		Bits
INL	Integral nonlinearity	Histogram method over full scale		±1.5	±3	LSB
DNL	Differential nonlinearity	Histogram method over full scale		±1	±2	LSB
Input Range			0		3.3	V
Input impedance				>1M		Ohms
FCLK	Clock rate	Successive approximation input clock rate		20		MHz
Input capacitance				5		pF
Number of channels				5		
Fsample	Sampling rate of each ADC			1		MSPS
F_input_max	Maximum input signal frequency			TBD		kHZ
I_active	Active supply current	Average for ADC during conversion		<0.9		mA
I_PD	Power-down supply current for core supply	Disable ADC		TBD		uA
Absolute offset error				TBD		mV
Gain error				TBD		%

9 PACKAGE INFORMATION

4 x 4 mm (body size), 0.4mm pitch QFN-32

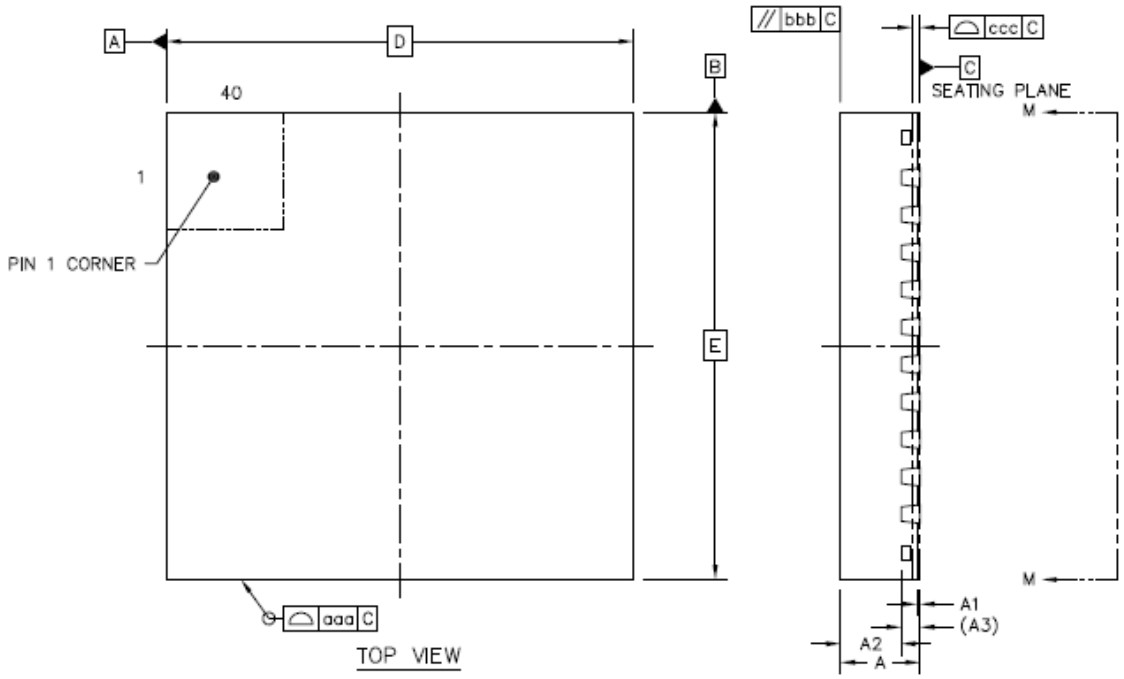


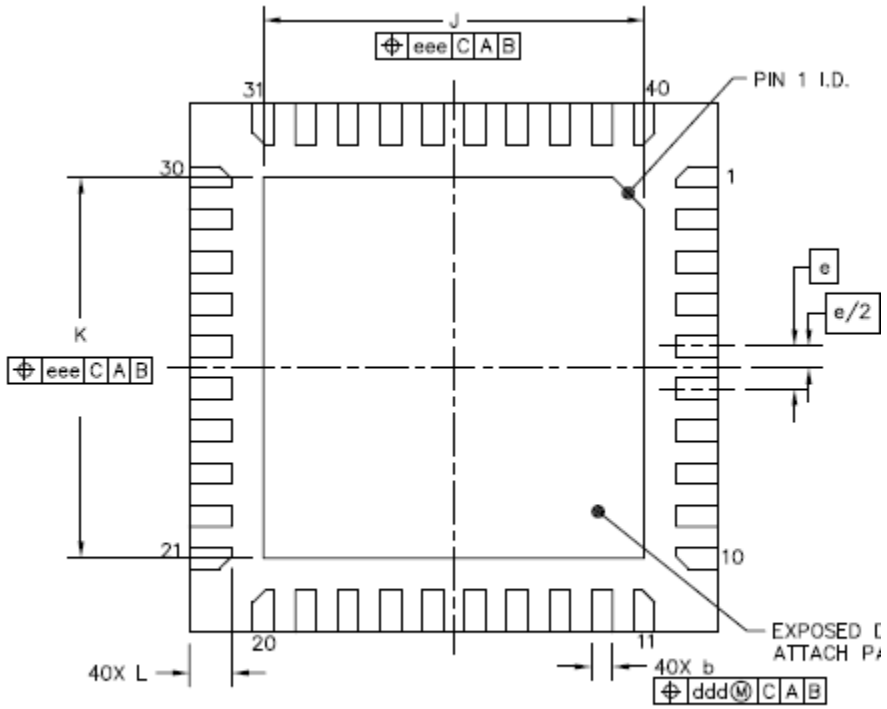


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	2.6	2.7	2.8
	Y	K	2.6	2.7	2.8
LEAD LENGTH		L	0.3	0.35	0.4
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure 16: QFN 4 x 4 mm Package Dimensions

5 x 5 mm (body size), 0.4mm pitch QFN-40

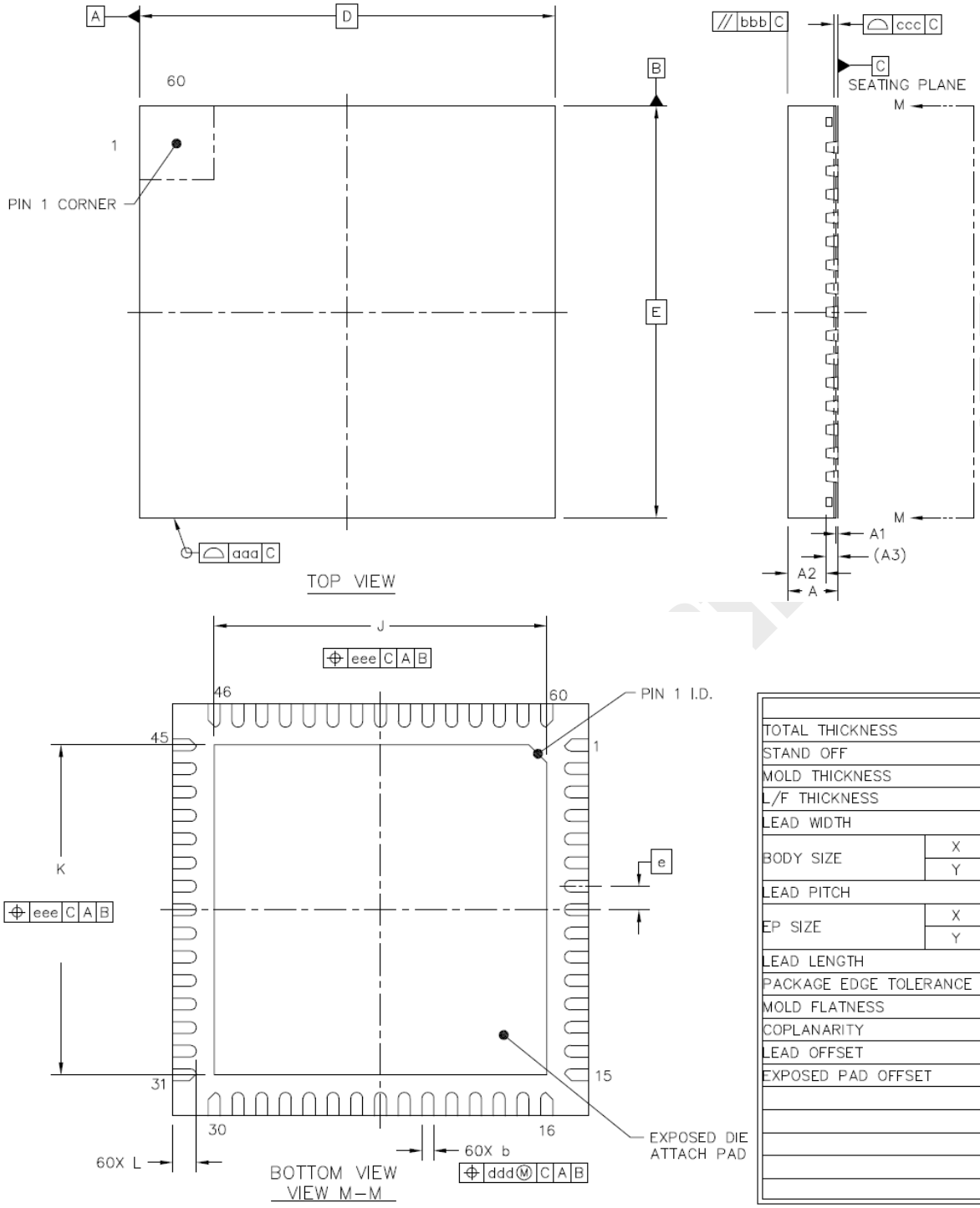




		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D	5 BSC		
	Y	E	5 BSC		
LEAD PITCH		e	0.4 BSC		
EP SIZE	X	J	3.5	3.65	3.8
	Y	K	3.5	3.65	3.8
LEAD LENGTH		L	0.3	0.4	0.5
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		bbb	0.1		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.1		
EXPOSED PAD OFFSET		eee	0.1		

Figure 17: QFN 5 x 5 mm Package Dimensions

7 x7 mm (body size), 0.4mm pitch QFN-60



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	5.5	5.6	5.7
	Y	K	5.5	5.6	5.7
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure 18: QFN 7 x 7 mm Package Dimensions

10 ORDERING INFORMATION

The table below provides the ordering information of the SV32WB0xx series of chips.

Table 30: SV32WB0xx Part Number

Part number	Category	Architecutre	Wireless Type	CPU CLKxSRAMxFlashxPackage		Feature	Operating Temp(°C)
SV32WB01	MCU/IoT	32 bit core	WiFi+BLE	320MHz x 384KB	16Mb x QFN32		-40 to +85
SV32WB01-L	MCU/IoT	32 bit core	WiFi+BLE	320MHz x 384KB	16Mb x QFN32	Lower power	-40 to +85
SV32WB01-T	MCU/IoT	32 bit core	WiFi+BLE	480MHz x 512KB	16Mb x QFN32	Turbo	-40 to +85
SV32WB01-H	MCU/IoT	32 bit core	WiFi+BLE	320MHz x 384KB	16Mb x QFN32	High Temp	-40 to +105
SV32WB05	MCU/IoT	32 bit core	WiFi+BLE	320MHz x 384KB	16Mb x QFN40		-40 to +85
SV32WB06	MCU/IoT	32 bit core	WiFi+BLE	480MHz x 512KB	NO x QFN60		-40 to +85
SV32WB07	MCU/IoT	32 bit core	WiFi+BLE	480MHz x 512KB	32Mb x QFN40		-40 to +85